

basic

620/i Software Data

The VDM BASIC programming system provides 620 computer users with a popular, easy-to-use programming language for a wide variety of business and scientific applications. The simplicity of VDM BASIC, plus its conversational operation, permit the inexperienced operator to perform useful programming with just a few hours of training. The computer responds to all commands entered by the user, thus reinforcing the learning process. If the operator makes an error, diagnostics report the type of error, and corrections can be made immediately.

For the experienced programmer, the VDM version of BASIC includes expanded instructions and capabilities. The advanced features permit programming a wider range of applications, yet the inherent simplicity of the language is retained.

Only 8K memory and a teletype are required for the use of VDM BASIC with any 620 system. Even dedicated 620 systems can be used to perform general computation when not used for other primary functions.

The distinguishing feature of VDM BASIC include:

- Arithmetic operators +, -, *, /, ↑
- Logical operators AND, OR, NOT
- Relational operators >, <, >=, <=
- Optional computed GOTO and GOSUB statements
- Parameter passing on GOSUB allowed
- SUB statement for defining parameters
- CALL statement for linking to assembler language subroutine
- Recursive execution of subroutines allowed
- STOP statement causes a program pause
- Complete matrix operations are provided

Operational features of the language are:

- Immediate syntax checking and diagnosis of statements
- Immediate, single statement execution when requested
- Dynamic assignment under program control of INPUT and OUTPUT devices (teletype, line printer, card reader, high speed paper tape, or magnetic tape)
- Program saving and restoring through secondary storage media

For additional information on VDM BASIC and other 620 software, contact:



varian data machines/The Big Company in Small Computers
2722 michelson drive / irvine / california / 92664 / (714) 833-2400

mos

620/i Software Data

Varian's Master Operating System (MOS) is a completely integrated software package which permits automated batch processing with Varian 620 series computers. All the stand-alone software features of the 620 computer are contained in MOS, plus the necessary software to integrate the package and interface it to the user's programs. MOS can be used with any 620 system equipped with 8K words of core memory, an ASR teletype, and a magnetic tape, rotating drum, or disc storage unit.

The Master Operating System provides centralized (teletype) control of the entire 620 system through the use of the following software modules:

- System Executive
- Input/Output Control System
- Resident Monitor
- System Loader
- DAS Assembler
- FORTRAN IV
- System Maintenance
- Edit and Debug
- Library

System modules process and execute the user's programs under the direction of the Executive (EXEC) routine. The EXEC interprets system directives and either executes the command directly, or calls and initiates the appropriate software module. When the sequence is completed, the EXEC again takes control and processes the next system directive.

The Input/Output Control System (I/OCS) processes all I/O requests. I/OCS achieves flexible, device-independent operation by assigning logical units (e.g., System File, System Input, and List Output) to peripherals instead of addressing the devices as specific hardware units. Assignments may be made up to a total of 255 logical units. These logical units are linked to physical devices through user directives and device assignment tables. These assignments may be changed at any time. This feature allows different physical peripheral devices to be substituted for I/O operations without requiring a costly reassembly of the program. The same peripheral can serve as more than one logical unit. I/OCS also permits use of multiple devices of a given type.

Input/Output operations for logical devices specified in I/O requests are serviced by I/O drivers. Only the drivers required for a given program are called into memory during run-time. Thus, memory utilization is optimized.

Under MOS supervision, the DAS Assembler and FORTRAN IV Compiler automatically process source statements to generate relocatable and compatible object programs. The FORTRAN IV run-time module contains arithmetic and mathematical function libraries.

Varian 620 object programs generated by the MOS assembler or FORTRAN IV compiler can be readily checked for program errors with the "Debug" MOS utility program. Its debugging capabilities include directives to search the entire memory for special values, to interrogate or change the MOS logical unit assignments, to execute a core dump, plus a multitude of other utility operations.

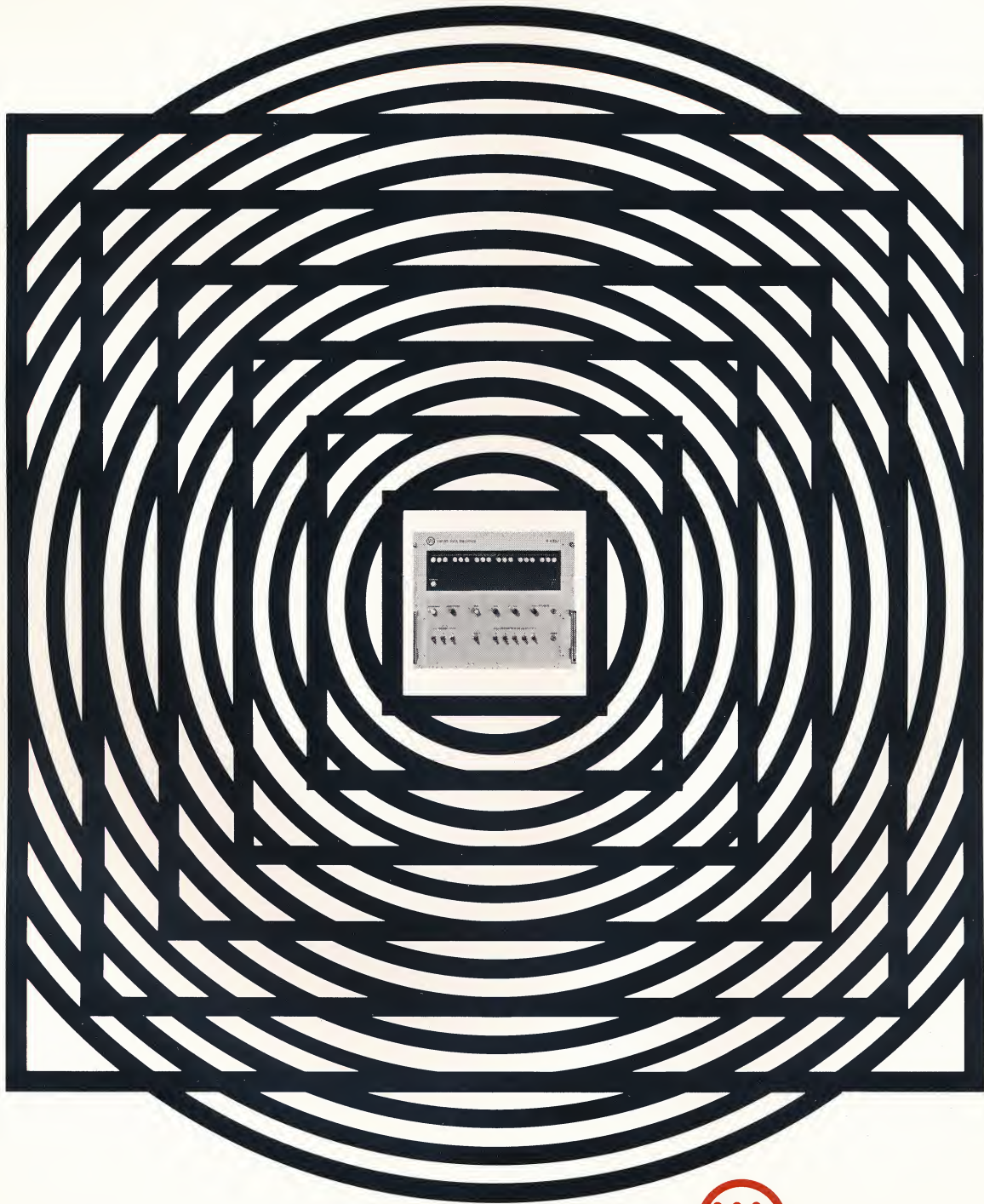
The System Maintenance program is designed for editing and reconfiguring the MOS library. Programs within the library may be added or deleted, using this feature. A Source Edit feature permits creation, duplication, and correction of 620 source files such as symbolic DAS and FORTRAN program statements.

For complete information on the Master Operating System and other 620 software, contact:

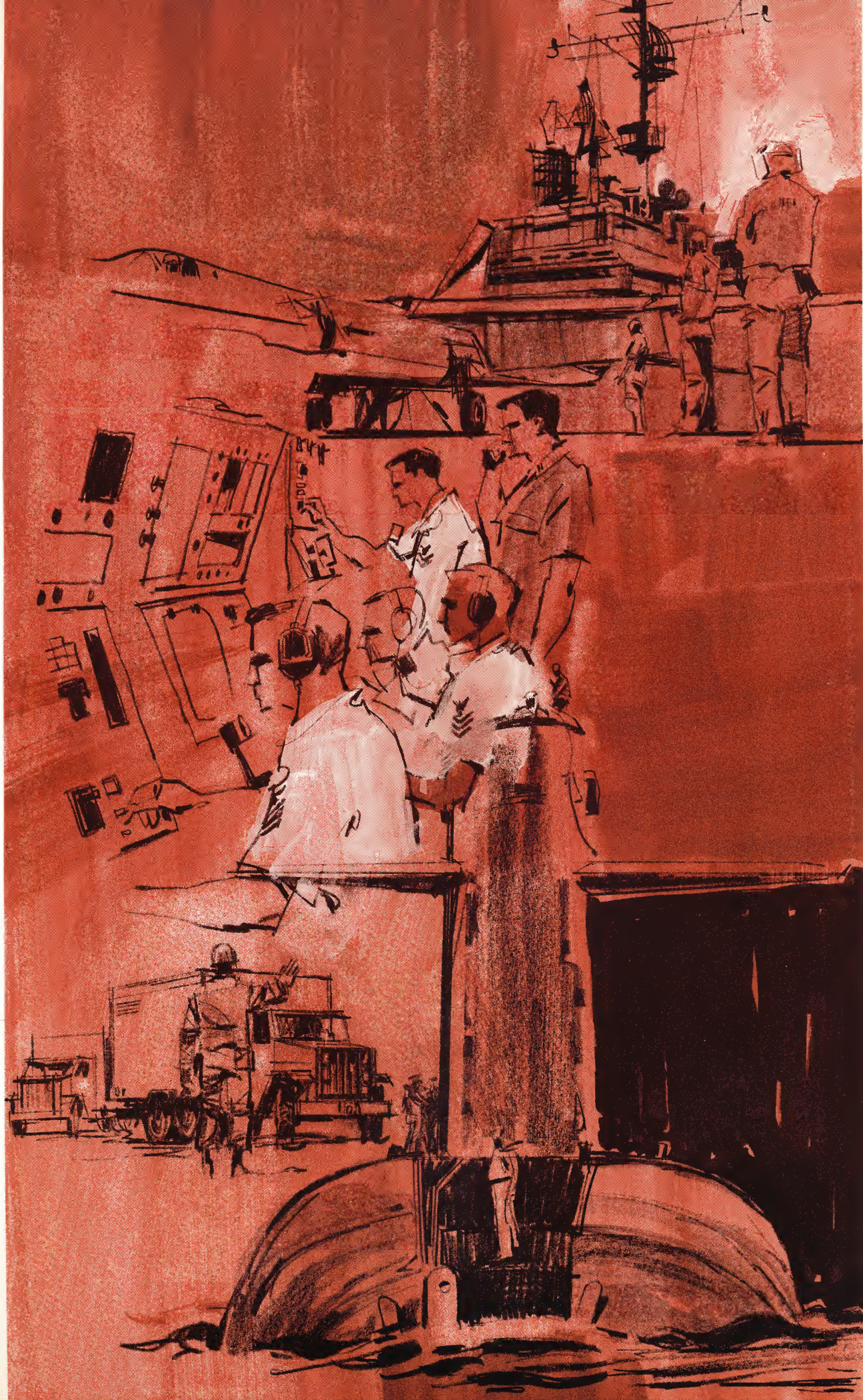


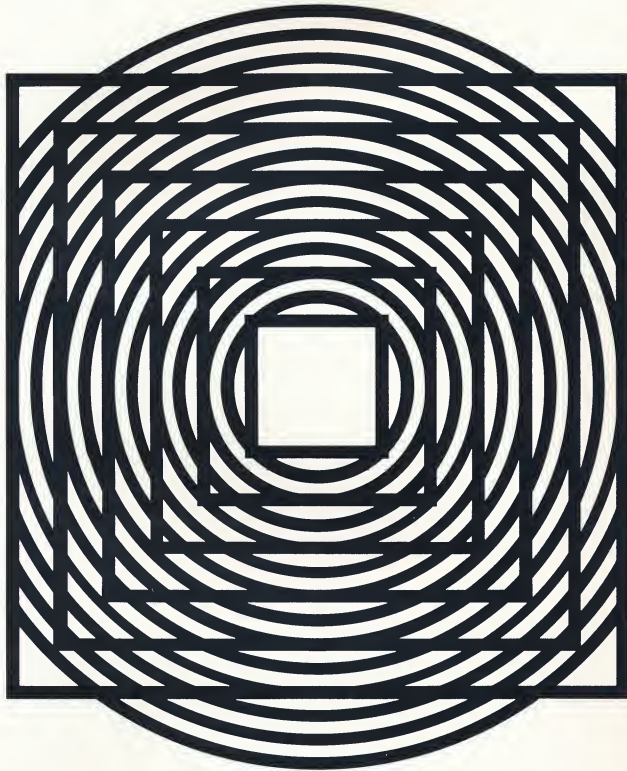
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varian
R-620/i
ruggedized
computer









varian R-620/i
the rugged
computer
for rugged
environments

The Varian R-620/i is a systems-oriented, general-purpose computer that has been designed for reliable operation in severe environments. It has been ruggedized specifically to counteract vibration, shock, humidity, and other environmental extremes.

At the same time, the Varian R-620/i is a versatile and powerful computer, featuring integrated-circuit reliability, easy interfacing, compact size, a choice of 16-bit or 18-bit precision, and a memory that can be expanded up to 32K words (8K in the main-frame chassis).

The Varian R-620/i can be mounted on trucks, installed on shipboard, or placed in a variety of other hazardous military or industrial environments.

Ceramic integrated circuits are used throughout the computer, and the assembled printed circuit boards are humi-sealed and treated to make them both corrosion and humidity resistant.

The environmental specifications to the left (underleaf) are an indication of the computer's ability to perform reliably even under conditions of shock and vibration. Certified tests have proved that even these figures are conservative.

To assure reliable operations in the presence of untrained or unauthorized personnel, data-safe key locks are provided on the front panel, and the front panel itself can be concealed or located up to 25 feet from the main frame of the computer.

The Varian R-620/i is functionally identical to the Varian 620/i, a widely used commercial computer. Software packages are interchangeable between the two computers. As a result, users of the ruggedized R-620/i can take direct advantage of the large library of software that has been field proven by the hundreds of Varian 620/i computers now in service.

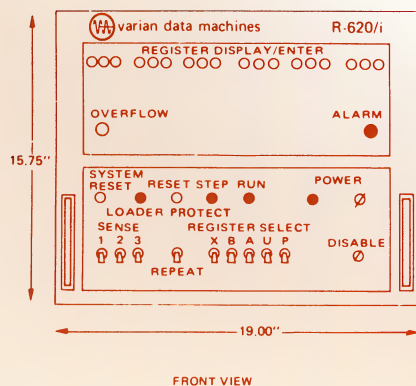
PERFORMANCE FEATURES:

- * Over 100 Basic Commands
- * 6 Addressing Modes
- * Expansion to 32,768 Words
- * 16-Bit or 18-Bit Words
- * 9 Hardware Registers
- * Comprehensive Software Library

ENVIRONMENTAL FEATURES:

- * High-Temperature Core Memory
- * Circuitry Protected Against Humidity
- * Vibration and Shock Resistant
- * Removable or Concealed Front Panel
- * Fits Standard RETMA Enclosure
- * Data-Safe Key Locks

varian R-620/i



... Internally Organized for Speed and Versatility

Nine hardware registers, organized with a unique bus structure and selection logic, give the Varian Data R-620/i its special computing power and programming flexibility.

The organization minimizes the programming required, minimizes the elapsed time between successive input and output transfers, and maximizes the I/O throughput of the computer.

Other valuable options include an elapsed-time meter and an operations monitor that sounds an alarm or initiates an interrupt whenever the computer is "trapped" in a sub-routine loop beyond a specified time limit. Contained within the mainframe is a power supply capable of operating the central processor plus all mainframe options, up to four I/O controllers and up to 8K of memory. The power supply can operate at 60 or 400 Hz, 110/220 volts (a voltage converter, operating off dc primary power, is available as an option.)

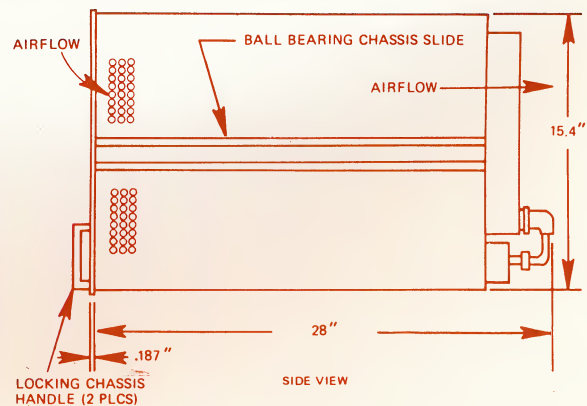
... Externally Designed for Ease of Operation and Servicing

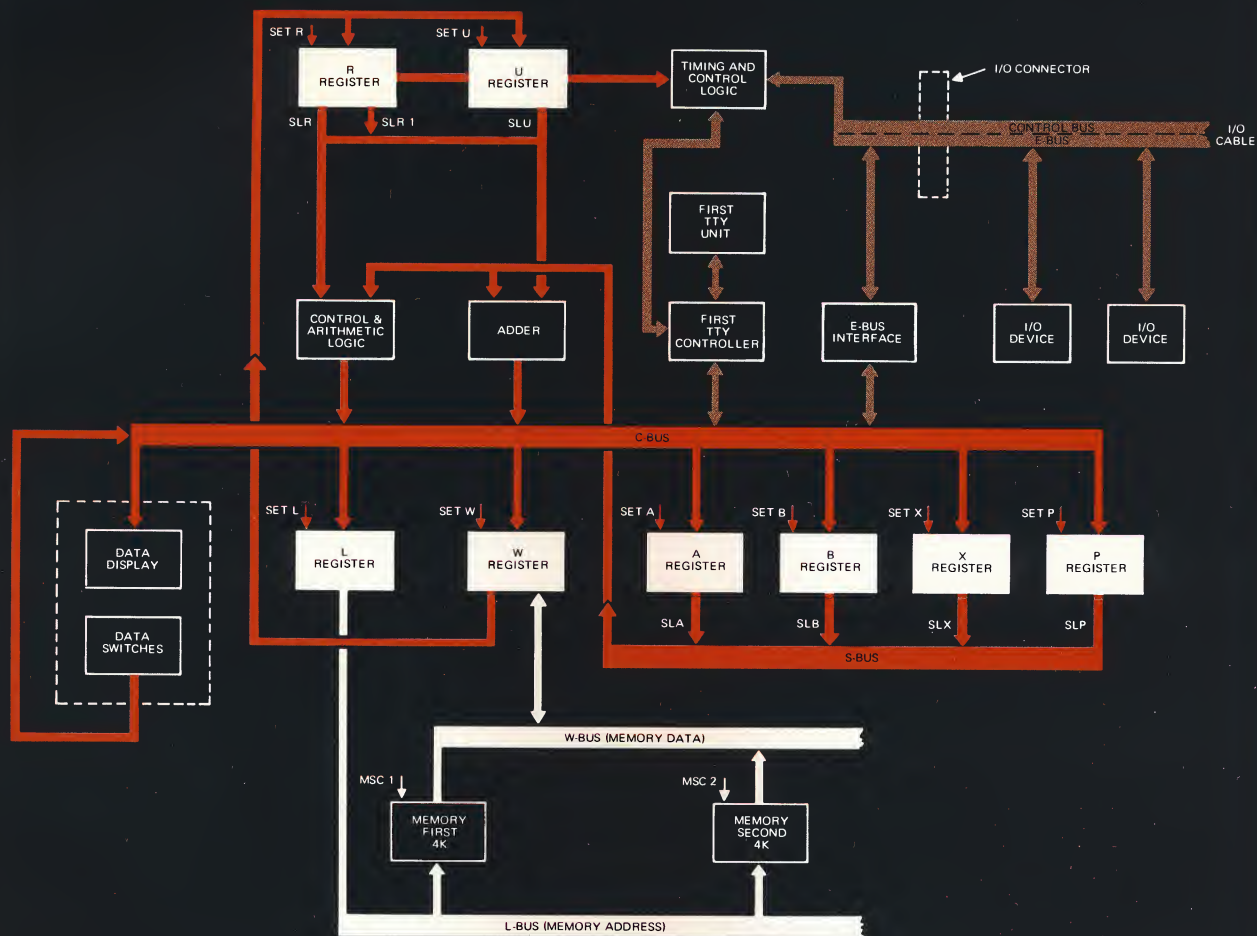
All controls are on the front panel for simple and reliable operation. In certain cases it may be desirable to conceal the panel or mount it remote from the main frame.

All system interconnects are attached to connectors on the back panel. I/O levels and logic are NPN, making the computer readily adaptable to nearly all peripheral devices and circuits.

The construction of the computer lends itself to logical troubleshooting procedures that, combined with diagnostic programs, simplify and speed any servicing that may be required. Repair time is minimized by simple replacement of modular sets of circuit cards. The central processor of the computer contains only 17 cards, 11 of which are unique.

Servicing of the computer is accomplished by extending the chassis on its slides and removing the top and bottom plates. All circuit cards are accessible from the top; the ground plane wiring is accessible from the bottom.





A REGISTER

A 16-bit or 18-bit register, serves as high-order half of accumulator and as source and destination for programmed input/output and micro-programming

B REGISTER

A 16-bit or 18-bit register, serves as the low-order half of accumulator, as a second hardware index register, and as a source and destination for programmed input/output

X REGISTER

A 16-bit or 18-bit register which permits indexing of memory addressing without adding time to accessing an indexed location

P REGISTER

A 16-bit or 18-bit register, serves as the program counter

U REGISTER

A 16-bit register, serves as a buffer for control unit, holds instruction being executed

S REGISTER

A 5-bit register (not shown) which, in combination with the U Register, controls the length of shift instructions

L REGISTER

A 12-bit register that holds the address of the memory location being accessed

W REGISTER

A 16-bit or 18-bit register that holds the word being transferred in or out of memory

R REGISTER

A 16-bit or 18-bit register which holds the multiplicand and divisor in arithmetic operations

L BUS

A 12-bit parallel communications path from the L Register to the address decoders in the memory modules

W BUS

A 16-bit or 18-bit parallel communications path from the W Register to the memory modules

C BUS

A 16-bit or 18-bit parallel communications path and selection logic for routing data between the arithmetic unit, the I/O bus and the operational registers

S BUS

A 16-bit or 18-bit parallel communications path and selection logic for routing data between the operational registers and the arithmetic unit

E BUS

A 16-bit or 18-bit parallel bi-directional "party line" I/O bus, includes the control lines for transfer ready, sense, control, interrupt address and acknowledge, and information entry

varian R-620/i specifications

TYPE

A system computer, general purpose digital, designed for on-line data system requirements, magnetic core memory, binary, parallel, single-address, with bus organization and micro-control.

MEMORY

Magnetic core, 16 bits (18 bits optional), 1.8 microseconds full cycle, 750 nanoseconds access time, 4096 words minimum expandable to 32,768 words.

ARITHMETIC

Parallel, binary, fixed point, 2's complement.

WORD LENGTH

16 bits standard; 18 bits optional.

SPEED (FETCH & EXECUTE)

Add or Subtract	3.6 microseconds
Multiply (optional)	18.0 microseconds, 16 bit
	19.8 microseconds, 18-bit
Divide (optional)	18.0 to 25 microseconds,
	16-bit
	19.8 to 28.8 microseconds,
	18-bit
Register change class	1.8 microseconds
Input/Output —	.
from A or B	3.6 microseconds
from memory	5.4 microseconds

OPERATION REGISTERS

A Register — accumulator, input/output, 16/18 bits.
B Register — double length accumulator, input/output, index register, 16/18 bits.
X Register — index register, 16/18 bits.
P Register — program counter, 16/18 bits.

BUFFER REGISTERS

R Register — operand register, 16/18 bits.
U Register — instruction register, 16 bits.
S Register — shift register, 5 bits, operates with the U Register for executing shift instructions.
L Register — memory address register
W Register — memory word register, 16/18 bits

CONTROL

ADDRESSING MODES

Direct addressing to 2,048 words
Relative to P Register 512 words
Index with X Register, hardware, does not add to execution time
Index with B Register, hardware, does not add to execution time
Multi-level indirect addressing
Immediate
Extended addressing (optional)

INSTRUCTION TYPES

Single word
Double word
Generic
Micro-command

INSTRUCTIONS: Over 100 standard commands, listed opposite, plus more than 128 macro-instructions:

3 Load
3 Store
5 Arithmetic (2 optional)
3 Logical
10 Jump
10 Jump and Mark
10 Execute
14 Immediate (2 optional)
13 Input/Output
26 Register Change
6 Logical Shift
6 Arithmetic Shift
2 Control
14 Extended Addressing (optional)
Over 128 micro-instructions

CONSOLE

Display and data entry switches for all operational registers, 3 sense switches, instruction repeat, single step; run; power on/off.

INPUT/OUTPUT

Processor Input/Output Options

Programmed Data Transfer
Single word to/from memory
Single word to/from A and B Registers
External control lines
External sense lines

Automatic Data Transfer

Direct memory access facility transfer with rates over 200,000 words per second.

Priority Interrupts

Group enable/disable, individually arm/disarm single instruction interrupt capability.

Real-Time Clock

Selectable time base.

Power Failure detect/restart

Interrupts on power failure and automatically restarts on power recovery.

MAINFRAME LOGIC AND SIGNALS

Integrated circuit, 8.8 MHz clock, logic levels 0 V false, +5 V true. External logic levels 0 V false, +3 V true.

R-620/i instruction list

Type	Mnemonic	Description	Time Cycles
Load	LDA	Load A Register	2
	LDB	Load B Register	2
	LDX	Load X Register	2
Store	STA	Store A Register	2
	STB	Store B Register	2
	STX	Store X Register	2
Arithmetic	ADD	Add to A Register	2
	SUB	Subtract from A Register	2
	INR	Increment and Replace	3
	MUL*	Multiply B Register, Double Length	10
	DIV*	Divide AB Register, Double Length	10-14
Logical	ERA	Exclusive OR to A Register	2
	ORA	Inclusive OR to A Register	2
	ANA	And to A Register	2
Jump	JMP	Jump UNCONDITIONALLY	2
	JOF	Jump if Overflow SET	2
	JAN	Jump if Register NEGATIVE	2
	JAZ	Jump if A Register ZERO	2
	JAP	Jump if Register POSITIVE	2
	JSS1	Jump if Sense Switch 1 is SET	2
	JSS2	Jump if Sense Switch 2 is SET	2
	JSS3	Jump if Sense Switch 3 is SET	2
	JXZ	Jump X Register ZERO	2
	JBZ	Jump B Register ZERO	2
Jump and Mark	JMPM	Jump UNCONDITIONALLY and Mark	2
	JOFM	Jump Overflow SET and Mark	2-3
	JANM	Jump A Register Negative and Mark	2-3
	JAZM	Jump A Register ZERO and Mark	2-3
	JAPM	Jump A Register Positive and Mark	2-3
	JS1M	Jump Sense Switch 1 SET and Mark	2-3
	JS2M	Jump Sense Switch 2 SET and Mark	2-3
	JS3M	Jump Sense Switch 3 SET and Mark	2-3
	JXZM	Jump X Register ZERO and Mark	2-3
	JBZM	Jump B Register ZERO and Mark	2-3
Execute	XEC	UNCONDITIONAL Execute	2
	XOF	Execute Overflow SET	2
	XAN	Execute A Register NEGATIVE	2
	XAZ	Execute A Register ZERO	2
	XAP	Execute A Register POSITIVE	2
	XS1	Execute Sense Switch 1 SET	2
	XS2	Execute Sense Switch 2 SET	2
	XS3	Execute Sense Switch 3 SET	2
	XXZ	Execute X Register ZERO	2
	XBZ	Execute B Register ZERO	2
Immediate	LDAI	Load A Register Immediate	2
	LDBI	Load B Register Immediate	2
	LDXI	Load X Register Immediate	2
	STAI	Store A Register Immediate	2
	STBI	Store B Register Immediate	2
	STXI	Store X Register Immediate	2
	ADDI	Add to A Register Immediate	2
	SUBI	Subtract from A Register Immediate	2
	MULI*	Multiply B Register Immediate	10
	DIVI*	Divide AB Register Immediate	10-14
	INRI	Increment and Replace Immediate	3
	ERAI	Exclusive OR to A Register Immediate	2
	ORAI	Inclusive OR to A Register Immediate	2
	ANAI	And to A Register Immediate	2
Input/Output	EXC	External Control Function	1
	CIA	Clear and Input to A Register	2
	CIB	Clear and Input to B Register	2
	CIAB	Clear and Input to A and B Registers	2
	INA	Input to A Register	2
	INB	Input to B Register	2

Type	Mnemonic	Description	Time Cycles
Register Change	INAB	Input to A and B Registers	2
	IME	Input to Memory	3
	OAR	Output A Register	2
	OBR	Output B Register	2
	OAB	Output OR of A and B Registers	2
	OME	Output from Memory	3
	SEN	Sense Input/Output Lines	2.25
	IAR	Increment A Register	1
	DAR	Decrement A Register	1
	IBR	Increment B Register	1
Logical Shift	DBR	Decrement B Register	1
	IXR	Increment X Register	1
	DXR	Decrement X Register	1
	CPA	Complement A Register	1
	CPB	Complement B Register	1
	CPX	Complement X Register	1
	TAB	Transfer AR to B Register	1
	TBA	Transfer BR to A Register	1
	TAX	Transfer AR to X Register	1
	TBX	Transfer BR to X Register	1
	TXA	Transfer XR to A Register	1
	TXB	Transfer XR to B Register	1
	TZA	Transfer Zero to A Register	1
	TZB	Transfer Zero to B Register	1
	TZX	Transfer Zero to X Register	1
	AOFA	Add OF to A Register	1
	AOFB	Add OF to B Register	1
	AOFX	Add OF to X Register	1
	SOFA	Subtract OF from A Register	1
	SOFB	Subtract OF from B Register	1
	SOFX	Subtract OF from X Register	1
Arithmetic Shift	SOF	Set Overflow	1
	ROF	Reset Overflow	1
	LSRA	Logical Shift Right AR k places	1 + .25 k
	LRLA	Logical Rotate Left AR k places	1 + .25 k
Control	LSRB	Logical Shift Right BR k places	1 + .25 k
	LRLB	Logical Rotate Left BR k places	1 + .25 k
	LLSR	Long Logical Shift Right k places	1 + .25 k
	LLRL	Long Logical Rotate Left k places	1 + .25 k
	ASRA	Arithmetic Shift Right AR k places	1 + .25 k
	ASRB	Arithmetic Shift Right BR k places	1 + .25 k
	ASLA	Arithmetic Shift Left AR k places	1 + .25 k
	ASLB	Arithmetic Shift Left BR k places	1 + .25 k
Arithmetic Shift	LASR	Long Arithmetic Shift Right k places	1 + .25 k
	LASL	Long Arithmetic Shift Left k places	1 + .25 k
Control	HLT	Halt	1
	NOT	No Operation	1

*Denotes optional instruction. Times given are for 16-bit computer. Add 1 cycle for each level of indirect addressing.



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varian Read-Only-Memory system

FEATURES

Nondestructive read out □ 350 nanoseconds cycle time □ 200 nanoseconds access time □ Interchangeable memory braid □ Output data register □ Up to 4,096 16-bit words (typical)

APPLICATIONS

In Computers — program storage; microprogram control; code conversion; stored tables; emulators □ In Displays — character generation □ In Communication Systems — code conversion □ In Machine Tool Control — storage of operating programs

Varian ROM (read-only memories) provide a flexible new approach to the architecture of memory systems for computers, data processors, machine tool controls, CRT displays, and a wide range of other digital data-processing devices.

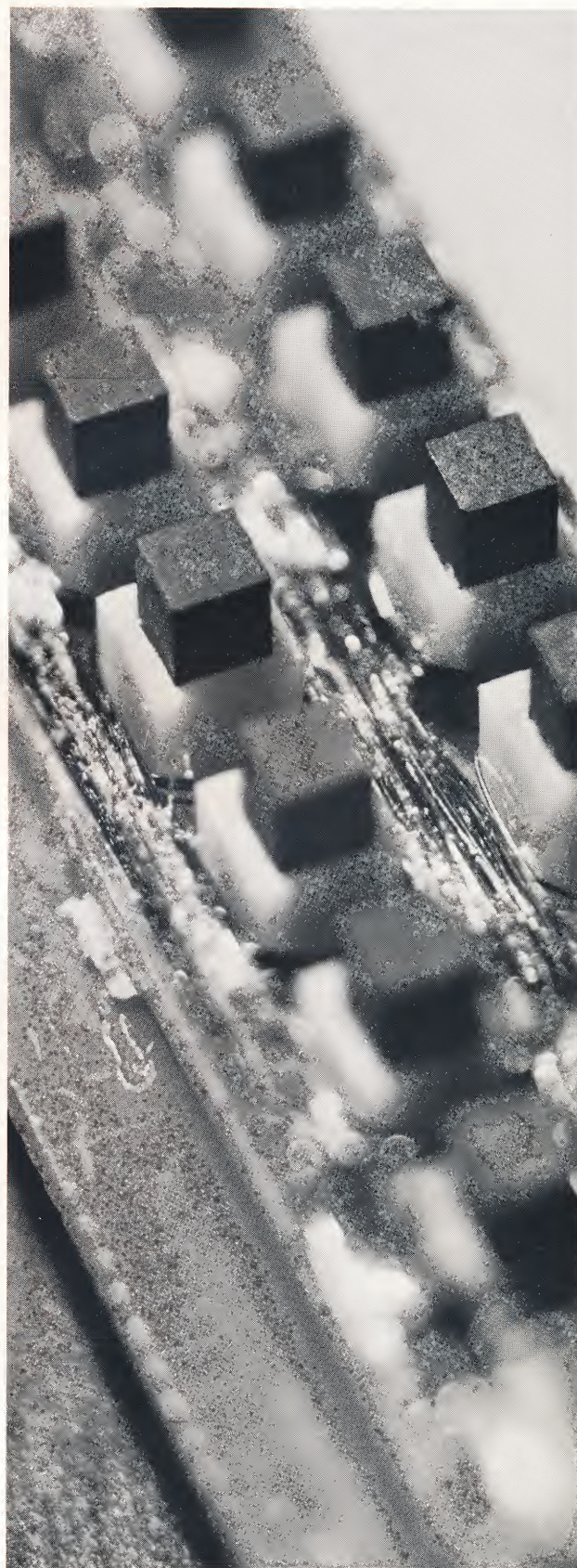
Fixed instruction subroutines, look-up tables, mathematical constants, and a variety of other information can be permanently stored in memory, yet accessed in a fraction of the time required by a standard core-memory system.

At the same time, Varian ROM's can be readily integrated into memory architectures based on the use of core memories as the principal data storage. Interface logic levels are identical to those in standard use, and an output register allows the data to be transferred according to the timing requirements of the overall system.

The bit values of the data stored in the Varian ROM systems are established by the arrangement of individual "word" wires, braided through or bypassing a series of ferrite transformer cores. The braided wires are laid in place at the time of manufacture or, if necessary can be changed in the field.

To meet changing short-term program requirements, however, the Varian ROM structure is designed so that the braided transformer cores are on a separate card from the circuit board carrying the principal ROM electronic elements. This provides a low cost and flexible method for changing the data contents. A library of braided-core cards can be kept on file, to be inserted into the ROM unit as required.

The Varian ROM design is adaptable to a wide range of word capacities and word lengths. Standard products in the Varian ROM line are described on individual data sheets. Standard word capacities are 128, 256, 512, 1,024, 2,048, and 4,096 word. Word length can range from 8 to 80 bits.



VARIAN ROM SYSTEMS

Varian ROM systems are based on the use of linear ferrite cores acting as transformers rather than as switchable cores. A "U" section and an "I" section combine to make up the complete transformer core structure.

The sense of each core (logic "1" or "0") is determined by braided wires that either pass through the core (logic "1") or bypass the core. Current flowing in a wire passing through a core induces a corresponding current in the secondary sense winding on that core (see drawing to the right). Current flowing through a wire that bypasses the core has no effect on the sense windings.

The braided wires, installed at the time of manufacture, determine the data content of the ROM, as specified by the user. A separate card (see opposite page) carries the braided wires and the U section of each core so that stored data can be quickly and economically altered as the program requirements change.

A typical block diagram and timing diagram for a Varian ROM are shown at the right. The system illustrated is for a 4,096-word ROM with a 16-bit word length.

The ROM circuitry consists of address decoders, transistor selection matrix, diode decode matrix, timing circuit, braid drive circuit, braided core matrix, sense amplifier, and an output data register.

Timing circuit consists of pulse signals that are triggered by the memory start and data strobe enable signals. Receipt of the pulse signals trigger the word current enable and data strobe pulse signals to enable the memory word lines and the output data register.

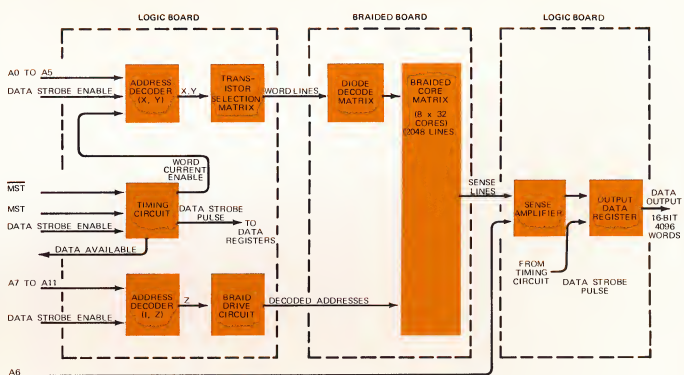
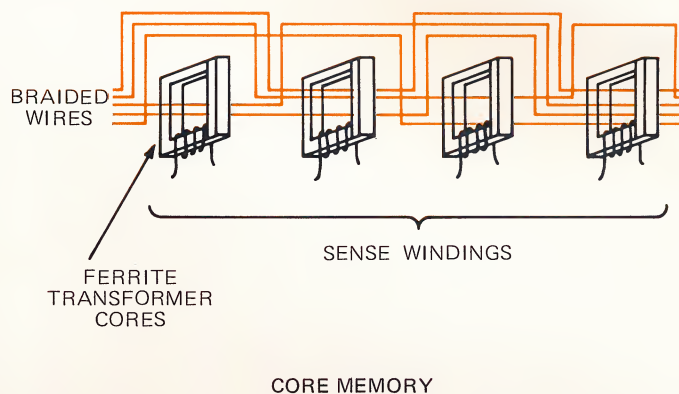
The data available pulse is also triggered to provide an output indication that the ROM is ready for data readout. These relationships are shown in the ROM timing diagram.

Word lines and decoded addresses are developed by the address decoder circuits from 12 address inputs (A0 to A12) except A6.

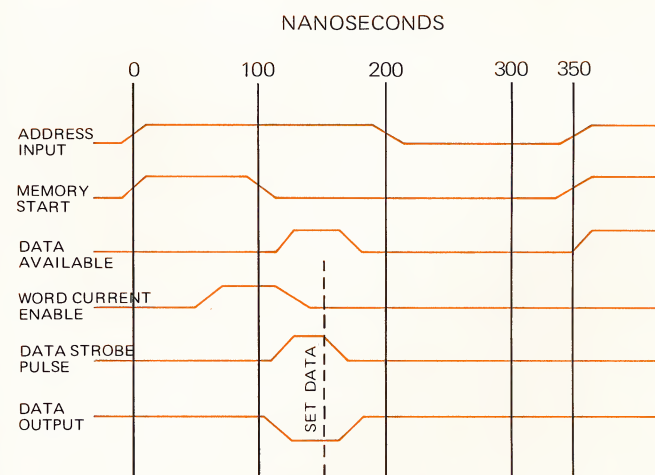
Interrogation of the ROM begins when the address decoders receive the memory start signal (MST). The core memory contains specific addresses of permanent binary data, stored as the result of the routing of 2,048 word lines through 8 x 32 ferrite transformer cores.

Control and timing for gating the core memory results in the output of 32-bits of data to the sense amplifier. Input address A6 is decoded and couples the selected word (half the 32 bits that are sensed) to the output data register.

The transition of the data strobe pulse from logic 1 to logic 0 sets the 16-bit output data register. The output information, on a selected word basis, is read out upon command during each read cycle.



BLOCK DIAGRAM

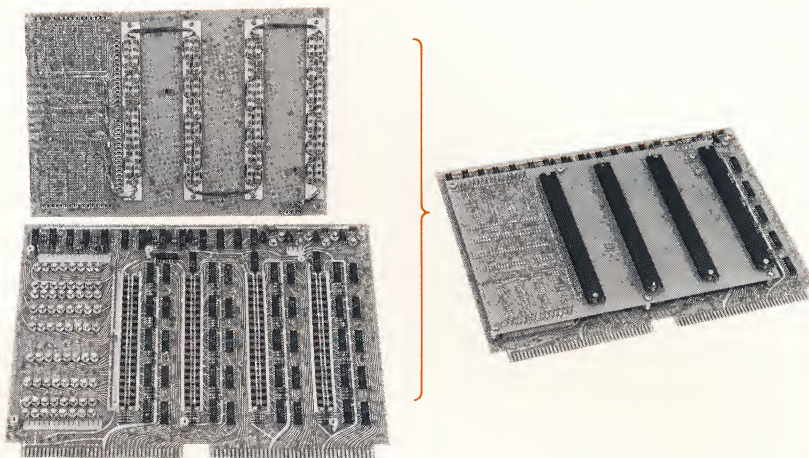


ROM TIMING DIAGRAM

INTERCHANGEABLE DATA BOARDS

The braided U-sections of the ferrite transformer core array are contained on a separate board attached to the logic board carrying the balance of the electronic circuitry. This allows the user to keep a library of braided core boards on file, each with a different data content. The data boards can be readily interchanged to meet various stored-program requirements.

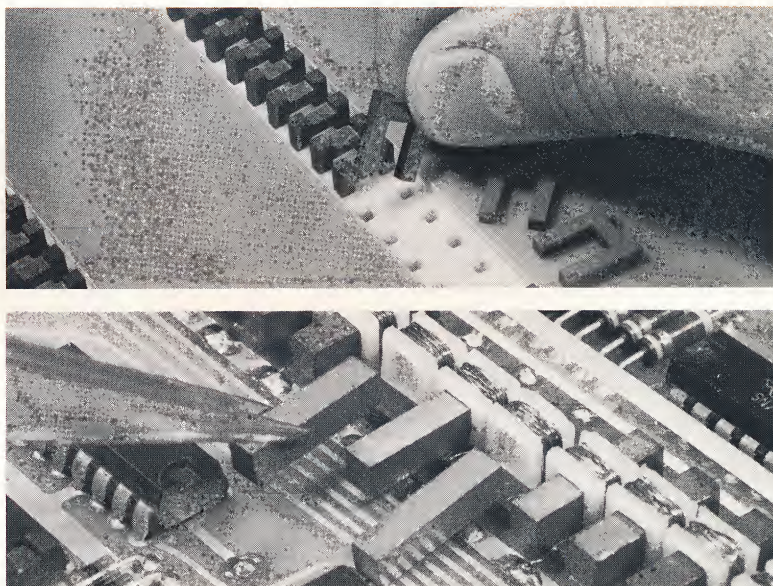
The photos to the right show the underside of the braided-core board, the top of the logic board, and the assembled ROM. Plastic covers on the top of the braided-core board hold the U sections of the ferrite cores in place.



SIMPLIFIED MAINTENANCE

Both the sense windings and the braided wires are separated from the ferrite cores by plastic sleeves so that if any core elements are accidentally damaged, they may be quickly and readily replaced without disturbing the balance of the system in any way.

The upper photo to the right shows a U section being replaced. The lower photo illustrates how an I section is inserted.



VARIAN ROM SPECIFICATIONS

The following specifications are for a typical Varian ROM system with a capability of storing 4,096 words, 16 bits per word. Specifications for ROM systems with other word capacities and bit lengths are available on request.

Memory Type	8 x 32 linear ferrite braided magnetic cores
Word Capacity	4,096 discrete addressable word locations
Word Length	16-bits
Cycle Time	350 nanoseconds
Access Time	150 nanoseconds
Logic Level	Input/Output: Logic "0" = -0.5V to +0.8V Logic "1" = +2.2V to +5.5V DTL and TTL compatible

Input Signal	12 high addressable lines
Output Signal	16-bits, 4,096 words
Size	15 x 15 inches
Power Requirements	+5V dc $\pm 5\%$ at 4 amperes
Environment	
Ambient Temperature	0°C to 50°C operating -25°C to 80°C non-operating
Relative Humidity	10 to 90% without condensation operating 10 to 95% without condensation non-operating
Shock and Vibration	Withstand normal shipping and handling site operation

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PRICE SCHEDULE
MAY 1, 1970

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